EP. 00 18404

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 2: G06F 9/12, 13/00; G11C 17/00; G05B 19/04

A1

(11) International Publication Number: WO 80/00383

(43) International Publication Date: 6 March 1980 (06.03.80)

(21) International Application Number: PCT/GB79/00136

(22) International Filing Date: 8 August 1979 (08.08.79)

(31) Priority Application Number: 33150/78

(32) Priority Date: 12 August 1978 (12.08.78)

(33) Priority Country: GB

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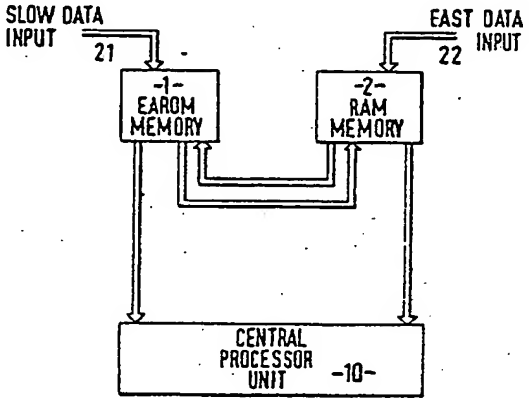
(81) Designated States: BR, CH (European patent), DE (European patent), DK, FR (European patent), GB (European patent), JP, NL (European patent), SE (European patent), US.

Published
With international search report

(54) Title: MEMORY SYSTEM FOR PROGRAMMABLE CONTROLLER



(57) Abstract

In a programmable controller having a central processor unit (10) and a memory, the invention provides the memory in the form of a fast memory (2) (suitably a RAM) and a slow memory (1) (suitably an EAROM). The processor is normally controlled by program, information in the slow memory. When it is desired to alter the control program, new program information is loaded into the fast memory. Control is then transferred to the fast memory, the new program information transferred to the slow memory, and control returned to the slow memory.

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MEMORY SYSTEM FOR PROGRAMMABLE CONTROLLER

This invention relates to a memory arrangement for a programmable controller.

In a programmable controller the central processor unit receives its control information from a memory in which the programme or programmes are stored. It is normal to prepare the programme off-line and thereafter transfer the programme to the processor memory.

Memories used in programmable controllers can be, amongst others, of the random access type (RAM) or can be of the electrically alterable read only type (EAROM). The former type has the advantage of relatively fast write and erase times but requires a power source in order that the information is retained. The EAROM memory is non-volatile i.e. no back-up batteries are required but suffers from the disadvantage that it has slow write and erase times when compared with the RAM memory. Thus, in programmable controllers which employ EAROM memories the facility for programming "on the fly" i.e. when the system is in use, is not available.

It is an object of the present invention to obviate or mitigate this disadvantage.

According to the present invention there is provided a memory system for a programmable controller, comprising a first memory connected to the central processor unit of the controller, a second memory connected in parallel to said first memory and connected also to said processor unit, the arrangement being such that data may be

transferred from the first memory to the second memory and vice-versa, that the central processor unit may receive information selectively from either the first memory or the second memory.

Preferably new data may be inserted in the first memory or in the second memory.

Preferably said first memory is of the electrically alterable read only type and said second memory is of the random access type.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of one memory arrangement according to the present invention;

Fig. 2 is a detailed circuit diagram of the EAROM memory part of a memory arrangement according to the present invention; and

Fig. 3 is a circuit diagram of the RAM memory part of a memory arrangement according to the present invention.

Referring to Fig. 1 a memory arrangement for a programmable controller comprises a first memory 1 of the electrically alterable read only type (EAROM) which contains a system programme which is fed to a central processor unit 10 of the programmable controller. New input data can be supplied to the memory 1 through a data bus 21. In view of the relatively slow write and erase times of the EAROM memory 1 the data bus 21 is termed a

slow data input.

A second memory 2 of the random access type (RAM) is provided and adapted to receive new programme or data through a data bus 22. The data bus 22 can be referred to as a fast data input in view of the relatively fast write and erase times of the RAM memory 2. The second memory 2 is connected to the first memory 1 so that the programme contained in the first memory can be substituted by the programme in the second memory 2. The second memory 2 is also connected to the central processor unit 10 and the programme in the second memory may also control the central processor, the first memory being at that time disabled or disconnected from the processor unit.

The second memory 2 being of the RAM type has relatively fast write and erase times and any alteration of the programme may be effected by entering data through the bus 22.

The inclusion of the second memory 2 of the RAM type allows a new programme to be inserted in the system whilst the system is operating under control of the first memory 1. Once the new programme has been inserted in the RAM memory 2 the processor can be controlled from this memory and simultaneously the new programme can be transferred to the EAROM memory 1. Additionally, the existing programme can be passed from the EAROM memory to the RAM memory for amendment whilst the processor is under the control of the memory 1.

Further, the arrangement of this invention allows the programme to be duplicated on to a number of EAROM memories which, because of their non-volatile nature, can be transferred to other systems without loss of information.

Still further, the above arrangement allows a number of new programmes to be tested without disturbing the existing system programme. This is effected by entering a new programme in the RAM memory 2 and controlling the system directly from the RAM memory 2, simultaneously disabling or disconnecting the system EAROM memory 1. After testing of the new or trial programme the system is returned to being controlled by the original programme in the EAROM memory 1.

Fig. 2 is a detailed circuit diagram the EAROM memory part of a memory arrangement of the present invention for application to a programmable controller.

Fig. 3 is a detailed circuit diagram of the RAM memory part of a memory arrangement of the present invention for application to a programmable controller.

CLAIMS

1. A memory system for a programmable controller having a central processor unit, a first memory connected to the central processor unit, a second memory connected to the central processor unit in parallel with said first memory, and means for transferring information between the first and second memories.

2. The memory system of claim 1, in which the first memory is a fast memory and the second memory is a slow memory.

3. The memory system of claim 2, in which the fast memory is a random access memory (RAM) and the slow memory is an electrically alterable read-only memory (EAROM).

4. The memory system of claim 3, in which the EAROM normally holds a system program, and the RAM is provided with a data bus input for loading new program information.

5. A method of operating a programmable controller having a central processor unit operating under the control of program information held in a memory, the method comprising providing the memory in the form of a fast memory and a slow memory, holding the program information in the slow memory for normal operation, loading new program information when desired into the fast memory, transferring control of the processor unit to the fast memory, transferring the new program information to the slow memory while control remains with the fast memory, and returning control to the slow memory.

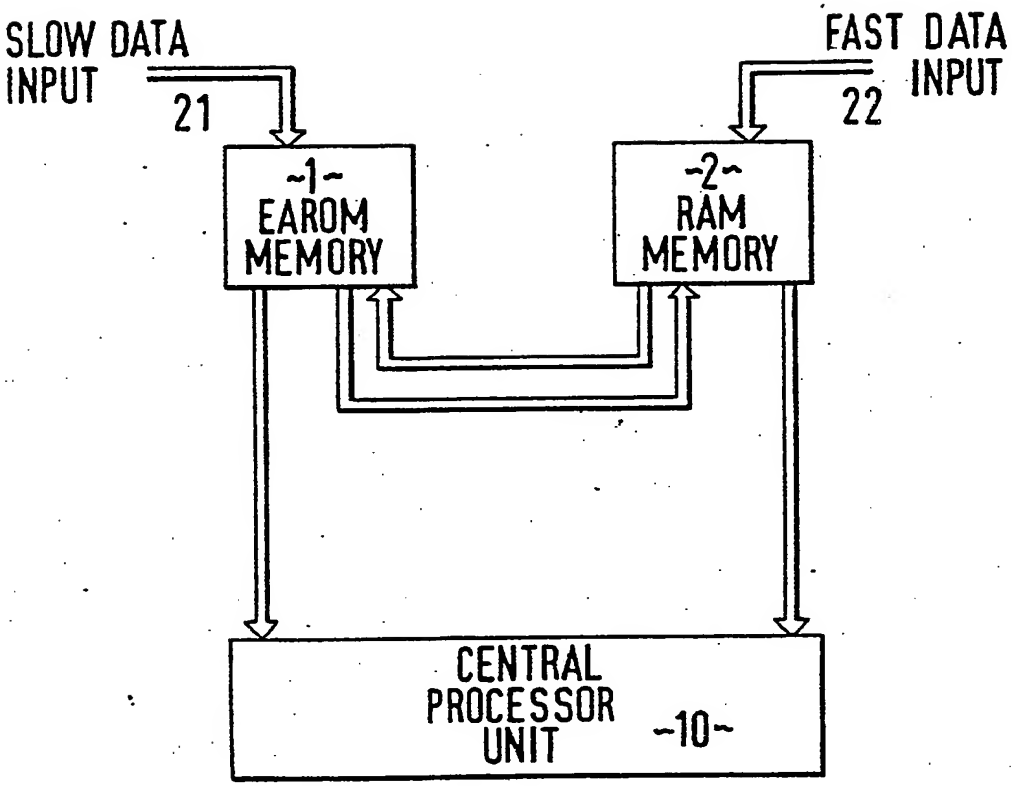

FIG. 1

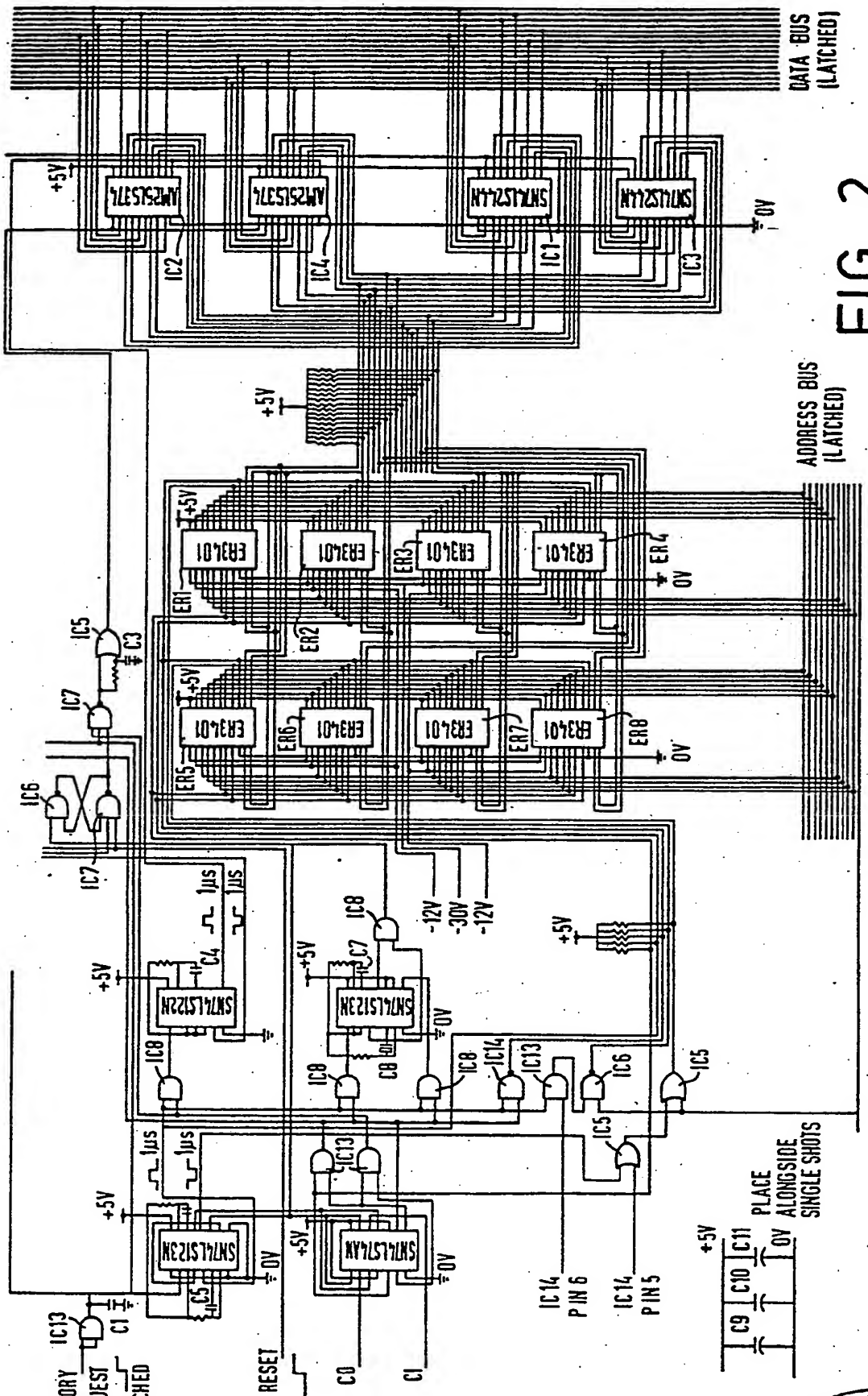

FIG. 2

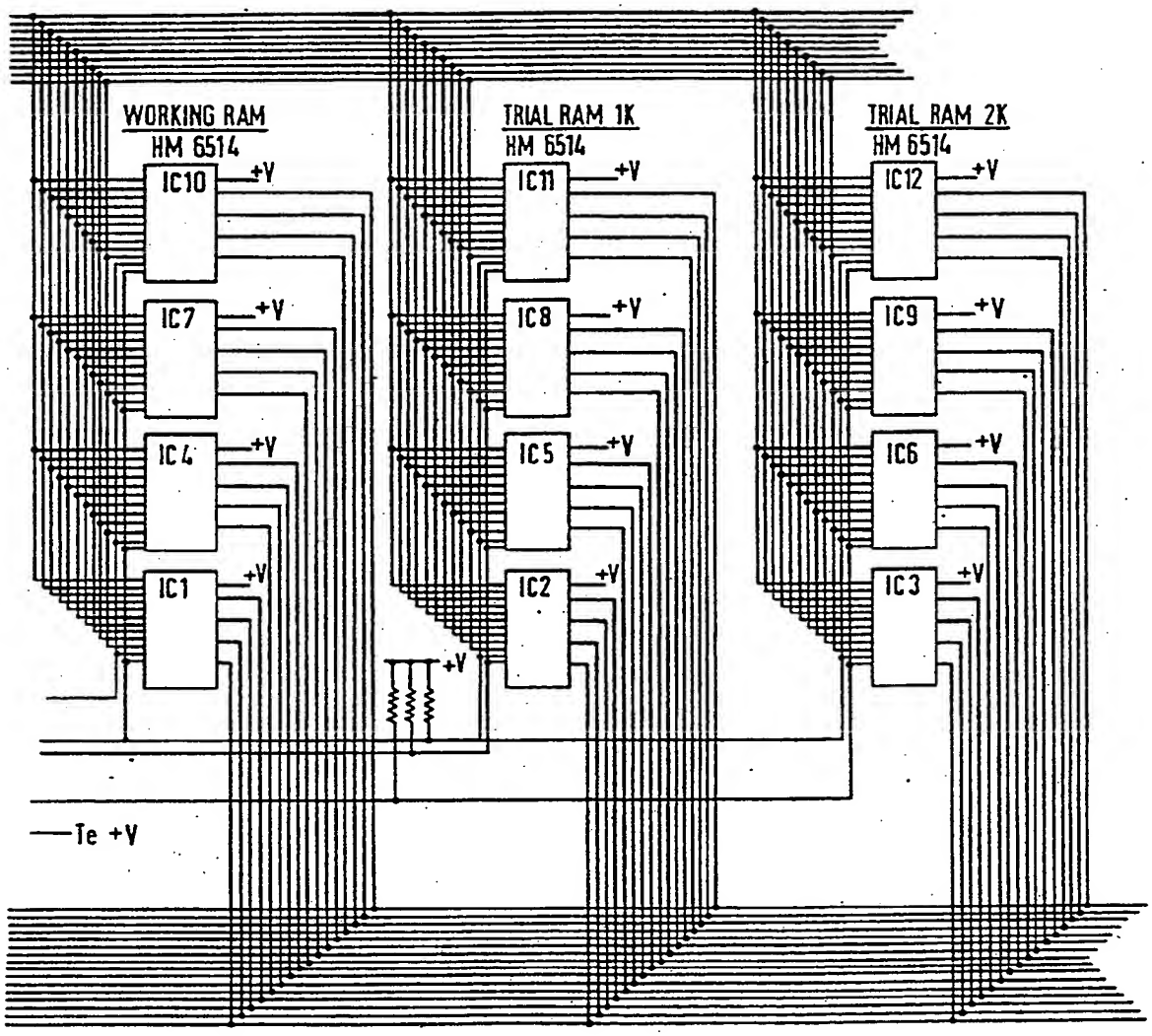

FIG. 3

INTERNATIONAL SEARCH REPO

International Application No PCT/GB 79/00136

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

G 06 F 9/12; G 06 F 13/00; G 11 C 17/00; G 05 B 19/04

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
Int.Cl.	G 06 F 9/12; G 06 F 13/00; G 11 C 17/00; G 05 B 19/04

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	FR, A, 2268304, published November 14, 1975, see claims 1,2, Toyoda-Koki	1-5
X	FR, A, 2291547, published June 11, 1976, see page 20, line 27 to page 22, line 33, Renault	1-5
X	FR, A, 2152564, published April 27, 1973, see page 2, lines 17-34, Allen Bradley	1-5
X	Proceedings of the sixth international Congress of Microelectronics. Documentation, München, 25-27 November 1974, published by Oldenbourg Verlag, München (DE) 8 pages, Weissberger: "User Microprogram Development For An LSI Processor", see page 5, first paragraph and from page 3, 4th paragraph to page 4, 2nd paragraph	1-5
X	DE, A, 2546713, published September 1, 1977, see page 3, last paragraph to page 4, 1st paragraph and figure 1, Ingentra	1-5

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* Special categories of cited documents: [15]

"A" document defining the general state of the art

"E" earlier document but published on or after the international filing date

"L" document cited for special reason other than those referred to in the other categories

"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
30th October 1979	9th November 1979
International Searching Authority [1]	**Signature of Authorized Officer [20]**
European Patent Office	G.L.M. KRUYDENBERG

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

X	Electronics, April 26, 1973, New-York (US) pages 116-119, Townsend: "Overlaid Memory simplifies programs has hidden nooks for diagnostics", see page 117, right-hand column, 3rd paragraph and page 118, left-hand column, 2nd and 3rd paragraphs	1-3
P	Microprocessors and microsystems, December 1978, pages 350 to 351, London (GB) Godliman: "Using EPROMs for File Storage", see page 351, left-hand column, last paragraph	1-5

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This International search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers _____, because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers _____, because they relate to parts of the International application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the International application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.